WHAT IS CLAIMED IS:

1. A non-volatile semiconductor device comprising:

a semiconductor substrate;

source and drain regions in said substrate separated by a channel region;

a gate comprising a layer of polycrystalline silicon of conductivity type different from that of said source and drain regions; and

a multilayer gate dielectric between said gate and said channel region comprising a charge storage layer having alterable charge storage properties by application of an electric field and having a dielectric thickness equivalent to that of a layer of silicon dioxide that is less than about 170 angstroms.

2. The device of claim 1 wherein said gate further comprises a layer of refractory silicide.

3. The device of claim 1 wherein said gate contains as few as $10^{11}/cm^3$ electrically active atoms of doping material.

4. The device of claim 3 wherein said conductivity types comprise a doping material selected from the group consisting of antimony, boron, phosphorus and arsenic.

5. The device of claim 1 wherein said source and drain regions are doped primarily N-type and said gate is doped P-type.

6. The device of claim 1 wherein said source and drain regions are doped primarily P-type and said gate is doped N-type.

7. The device of claim 1 wherein said multilayer gate dielectric further comprises a second dielectric material layer between said charge storage layer and said channel.

8. The device of claim 7 wherein said second dielectric material layer comprises silicon dioxide.

9. The device of claim 7 wherein said multilayer gate dielectric further comprises a third dielectric material layer between said charge storage layer and said gate.

10. The device of claim 9 wherein said third dielectric material layer comprises silicon dioxide.

11. The device of claim 9 wherein said third dielectric material layer comprises a three layered structure of a layer of silicon dioxide, on a layer of silicon nitride on yet another layer of silicon dioxide.

12. The device of claim 1 wherein said charge storage layer comprises a floating gate.

13. The device of claim 12 wherein said floating gate comprises polycrystalline silicon.

14. The device of claim 1 wherein said charge storage layer comprises a dielectric material capable of trapping charge carriers.

15. The device of claim 1 wherein said charge storage layer comprises a dielectric material capable of trapping charge polarization.

16. The device of claim 1 wherein said charge storage layer comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and ferroelectric materials.

17. The device of claim 1 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a second conductivity type.

18. The device of claim 1 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a first conductivity type; and

wherein said non-volatile memory device further comprises a first well region of a second conductivity type formed in said substrate as to surround at least said source and drain regions and said channel region.

19. The device of claim 1 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a second conductivity type; and

wherein said non-volatile memory device further comprises a first well region of a first conductivity type formed in said substrate as to surround at least said source and drain regions and said channel region; and

wherein said non-volatile memory device further comprises an additional second well region of the second conductivity type formed in said substrate as to surround at least said first well region.

20. The device of claim 1 wherein said channel region comprises a buried channel.

21. The device of claim 1 wherein said channel region comprises a depletion channel.

22. A non-volatile semiconductor device comprising:

a semiconductor substrate;

source and drain regions in said substrate separated by a channel region having a channel length less than about 0.7 microns;

a gate comprising a layer of polycrystalline silicon of conductivity type different from that of said source and drain regions; and

a multilayer gate dielectric between said gate and said channel region comprising a charge storage layer having alterable charge storage properties by application of an electric field.

23. The device of claim 22 wherein said gate further comprises a layer of refractory silicide.

24. The device of claim 22 wherein said gate contains more than $10^{11}/cm^3$ electrically active atoms of doping material.

25. The device of claim 24 wherein said conductivity types comprise a doping material selected from the group consisting of antimony, boron, phosphorus and arsenic.

26. The device of claim 22 wherein said source and drain regions are doped primarily N-type and said gate is doped P-type.

27. The device of claim 22 wherein said source and drain regions are doped primarily P-type and said gate is doped N-type.

28. The device of claim 22 wherein said multilayer gate dielectric further comprises a second dielectric material layer between said charge storage layer and said channel.

29. The device of claim 28 wherein said second dielectric material layer comprises silicon dioxide.

30. The device of claim 28 wherein said multilayer gate dielectric further comprises a third dielectric material layer between said charge storage layer and said gate.

31. The device of claim 30 wherein said third dielectric material layer comprises silicon dioxide.

32. The device of claim 30 wherein said third dielectric material layer comprises a three layered structure of a layer of silicon dioxide, on a layer of silicon nitride on yet another layer of silicon dioxide.

33. The device of claim 22 wherein said charge storage layer comprises a floating gate.

34. The device of claim 33 wherein said floating gate comprises polycrystalline silicon.

35. The device of claim 22 wherein said charge storage layer comprises a dielectric material capable of trapping charge carriers.

36. The device of claim 22 wherein said charge storage layer comprises a dielectric material capable of trapping charge polarization.

37. The device of claim 22 wherein said charge storage layer comprises a material selected from the group consisting of silicon nitride, silicon oxynitride, silicon-rich silicon dioxide, and ferroelectric materials.

38. The device of claim 22 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a second conductivity type.

39. The device of claim 22 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a first conductivity type; and

wherein said non-volatile memory device further comprises a first well region of a second conductivity type formed in said substrate as to surround at least said source and drain regions and said channel region.

40. The device of claim 22 wherein said substrate has a first conductivity type and said source and drain regions are semiconductor regions of a second conductivity type; and

wherein said non-volatile memory device further comprises a first well region of a first conductivity type formed in said substrate as to surround at least said source and drain regions and said channel region; and

wherein said non-volatile memory device further comprises an additional second well region of the second conductivity type formed in said substrate as to surround at least said first well region.

41. The device of claim 22 wherein said channel region comprises a buried channel.

42. The device of claim 22 wherein said channel region comprises a depletion channel.

43. A non-volatile semiconductor device having source and drain regions of first conductivity type in said substrate separated by a channel region of length less than about 0.7 microns, comprising:

a gate comprising a layer of polycrystalline silicon of second conductivity type different from that of said first conductivity type; and

a multilayer gate dielectric between said gate and said channel region comprising a charge storage layer having alterable charge storage properties by application of an electric field.

44. The non-volatile semiconductor device of claim 43 wherein said gate dielectric has a dielectric thickness equivalent to that of a layer of silicon dioxide that is less than about 170 angstroms.

45. The device of claim 43 wherein said gate further comprises a layer of refractory silicide.

46. The device of claim 43 wherein said source and drain regions are doped primarily N-type and said gate is doped P-type.

47. The device of claim 43 wherein said source and drain regions are doped primarily P-type and said gate is doped N-type.

48. The device of claim 43 wherein said charge storage layer comprises a floating gate.

49. A method for making a non-volatile semiconductor device comprising:

forming a multilayer gate dielectric having a charge storage layer with alterable charge storage properties by application of an electric field, and having a dielectric thickness equivalent to that of a layer of silicon dioxide that is less than about 170 angstroms;

forming a gate comprising polycrystalline silicon of first conductivity type on said gate dielectric; and

forming source and drain regions separated by a channel region in a semiconductor substrate, said source and drain regions having a second conductivity type different from said first dielectric type.